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Analysis of a Novel Four Level Flying Capacitor H – Bridge Converter

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ABSTRACT. In this paper, a novel four-level flying capacitor inverter and its comparison with the conventional flying capacitor topology in terms of THD analysis are proposed. This new topology have some advantages over conventional one as following: The blocking voltages are the same for all switches used in the configuration, there is no need for capacitor midpoint connection and this eliminates low frequency current which circulate in dc-link capacitors, and the number of flying capacitor is reduced as compared with conventional form of it. The operation of the topology, modulation strategy, simulation results, and THD analysis for the output waveforms are presented in this paper.

Keywords: Flying capacitor, H-bridge, Inverter, Four-level topology, THD

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1. Introduction

While the need for electricity grows from day to day in many countries, researchers have started to focus on converting it more and more efficiently. For this reason, multilevel converters have attracted notice a lot in technical literature for last decades (Prabaharan and Palanisamy 2017). Although the term of multilevel converter is used frequently as different terminology utilization in the research area of power electronics, it might be sometimes confusing for the people who are not familiar with this topic in detail. In order to overcome this confusion, Akagi presented a chronological overview for multilevel converter topologies in (Akagi 2017).

When multilevel converters were first presented in the area, their advantages, such as smaller common-mode (CM) voltage, lower switching frequency, and less distortion in output voltages - input current dominated the usage of classical two-level topologies (Rodriguez *et al.* 2002, Gautam *et al.* 2017). The strong motivation behind the endeavor for developing multilevel converter topologies are to bloom modulation methods, balance the DC link's voltage, and make the value of total harmonic distortion (THD) better (Joca *et al.* 2012).

Multilevel inverter configurations have started to be employed in low power levels as well, especially for single-phase applications. Some examples can be given as followings: A single-phase multilevel converter for electrified railway (Rahmani and Al-Haddad 2006) and a new family of single-phase multilevel inverters without clamping diodes and capacitors (Chen *et al.* 2008). It has been shown that THD is a significant factor to evaluate the performance of the topologies (Daher and Antunes 2008, Radermacher *et al.* 2004).

Although there are some applications for lower power levels in this area as stated above, most of researches have been made for high power implementations. One of its possible reasons is stated in (Sathiyanarayanan and Kumar 2013) as the increase for the size of wind turbines due to the generation of more energy and the cost reduction as well. Besides the dominance of high power applications in literature, the lower ones also have drawn interest of researchers when off-grid systems are taken into consideration. Therefore, as the main contribution of this study; it is aimed that improving a low-power-level multilevel inverter which can be employed in small wind turbines or solar power systems for residential or small business utilization.

Among the multilevel inverter topologies, the flying capacitor topology has some benefits over others as followings: There is no need for clamping diodes which limit the voltage across the switches, isolated DC voltage sources are not demanded, voltage unbalance

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doesn't occur in bus capacitors, and capability of operating in a wide range of modulation strategies.

In this paper, a comparison between conventional four-level flying capacitor topology and four-level flying capacitor H-bridge topology in (Dos Santos *et al.* 2014) is explored for the output waveforms in terms of THD analysis. In the second section, the structures and the modulation techniques of converters which are subject to compared in this study. It continues with THD values and analysis of the output waveforms accompanied with simulation results in third section. Finally, conclusion section is given and the paper is completed.

2. Flying Capacitor Converter Topologies

2.1 The structure and modulation technique of conventional four-level flying capacitor inverter

In Fig. 1, the structure of conventional four-level flying capacitor inverter is illustrated. Totally, six switching devices and two flying capacitors are used in this topology. Four level stepped waveform is basically formed as following: With the change of switching states of semiconductor device, flying capacitor C_1 is used to generate two-level waveform; C_2 is for three-level signal of output; and the leg of connection to two DC sources is used to consist four-level output voltage. This configuration and its operation was explained explicitly in (Lai and Peng 1996) with all details. In this paper, one phase of the conventional four-level flying capacitor inverter's structure, which is shown in Fig. 1, is used for simulation.

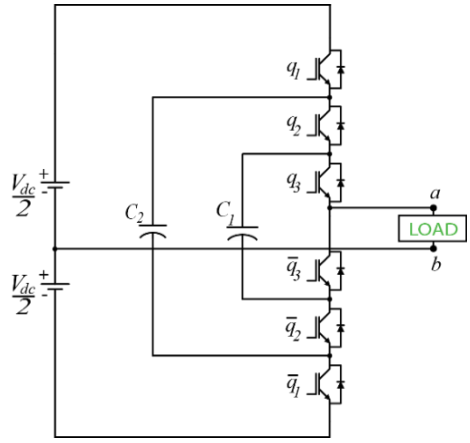

Fig. 1 The structure of conventional four-level flying capacitor inverter.

Multicarrier sinusoidal PWM technique, based on level shifted method, is used as the modulation strategy for this conventional four-level flying capacitor inverter topology. In this approach, totally three triangular carrier signals are compared with one reference sinusoidal signal. As shown in Fig. 2, those triangular signals are located in the same phase but different levels.

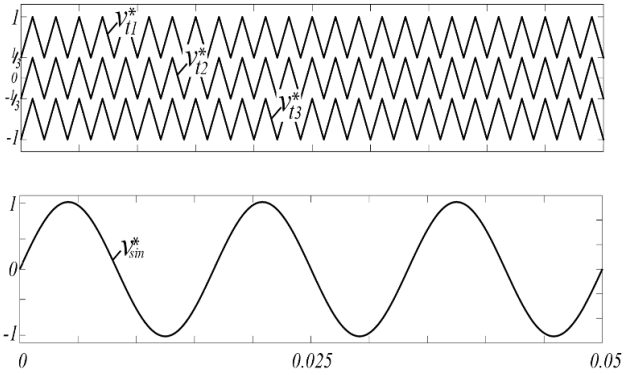

Fig. 2 Waveforms of carrier and reference signals.

In order to make the topologies of flying capacitor inverters worked properly, there is a need for keeping their capacitor voltages at certain values, which are actually their nominal magnitudes. Since such a topology has its own faults and instability, especially during reactive power flow circumstances, the capacitor voltages might deviate in steady-state and transient periods. To balance these voltages of flying capacitors, mainly three methods are proposed in literature: Open-loop control methods, employment of extra power circuitry in addition to open-loop control, and closed-loop methods (Choi and Saeedifard 2012). None of the methods have been used in the implementation of conventional four-level flying capacitor configuration for this study, because this is not within the scope of aims in this article. Instead, the best result is obtained from simulation during its transient condition to make a comparison with the proposed topology given in next topic.

2.2. Four-level flying capacitor h-bridge inverter topology

Beside the high and medium power systems, DC-AC multilevel inverters for single phase applications has been explored in literature due to its importance in low power applications well. For this reason, a new flying capacitor inverter topology shown in Fig.3 is presented in (Radermacher *et al.* 2004). Such a topology can operate either with three separate DC sources, which can be obtained through a set of PV arrays, or from a unique DC source with additional circuitry. This topology proposes some advantages over conventional one as following: The blocking voltages are the same for all switches used in the configuration, there is no need for capacitor midpoint connection and this eliminates low frequency current which circulate in dc-link capacitors, and the number of flying capacitor is reduced as compared with conventional form of it.

The modulation strategy for this converter, which is shown that in Fig. 4, can be assumed as a combination of two- and three-level PWM approaches: One triangular carrier signal is used for the two-level leg and the other two one is for three-level leg. The analog implementation of PWM approach for the proposed converter is illustrated in Fig. 4. Since each leg is

capable to synthesize different values of voltages, such as $2V_{dc}$ for two-level leg and $4V_{dc}$ for the three-level leg, the sinusoidal waveforms used to define PWM signals should follow the same ratio. Indeed, there is a requirement to accomplish this rule: The reference voltage for the three-level leg is twice bigger than two level leg.

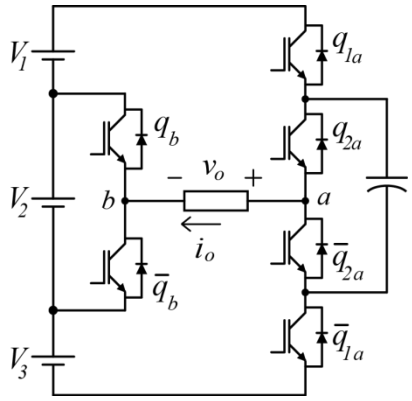

Fig. 3 Four-level flying capacitor h-bridge inverter topology

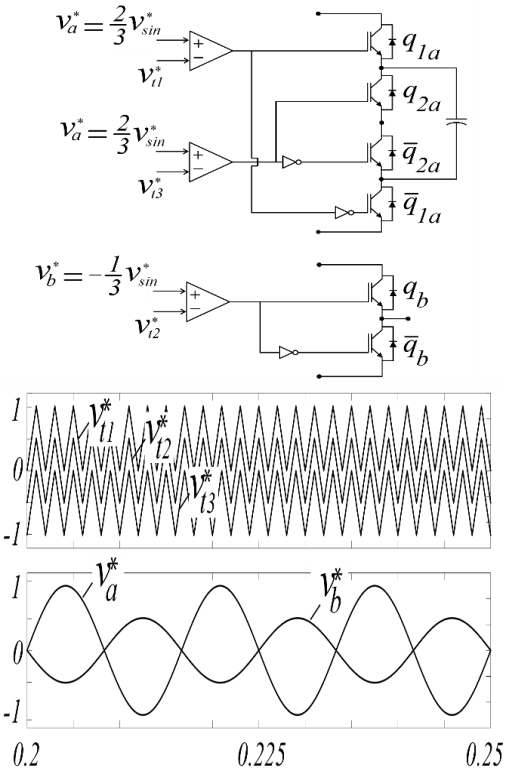

Fig. 4 Analog implementation of modulation strategy with carrier and reference signals.

Considering all possibilities of switching states available in this topology which is depicted in Fig. 3, the output voltage is determined by Table 2. There are totally eight states for this topology which consists of three switching device and three its complementary ones. However, two states are forbidden because current does not find any way to go through the circuit, so those two states are not shown in the table.

Table 1.
Output voltages considering all switching states available.

State	{q_{1a} q_{2a} q_b}	v_o
1	{0 0 0}	$-V_{dc}$
2	{0 0 1}	$-3V_{dc}$
3	{0 1 0}	$-V_{dc}$
4	{0 1 1}	V_{dc}
5	{1 1 0}	$3V_{dc}$
6	{1 1 1}	V_{dc}

As observed in Fig. 3, the single-phase load is connected between the points a and b of converter, which leads to an output voltage given by:

$$v_0 = (2q_{1a} + 2q_{2a} - 2q_b - 1)V_{dc} \quad (1)$$

Although a detailed analysis voltage balancing of flying capacitor for this topology is not investigated in this paper, it can be stated briefly that there is a natural balancing for the flying capacitor. Indeed, voltage of the flying capacitor have small ripples and almost a constant particular value during the simulation of this topology.

Each state, given by Table 1, has two topological circuits for both positive and negative currents as shown in Fig. 5 for states 3 and 4.

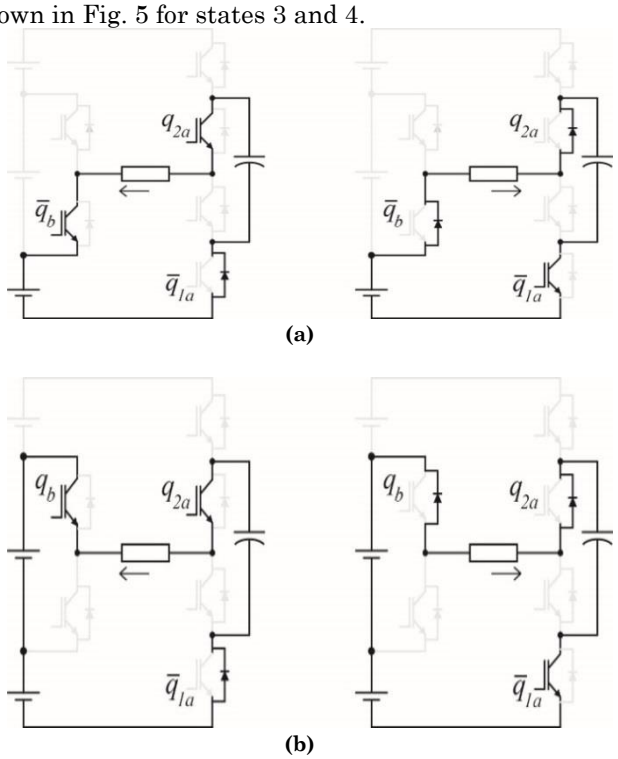

Fig. 5 Topological states in positive and negative currents of **(a)** state 3 and **(b)** state 4.

From the figures of topological states, it is understandable how flying capacitor is charged and discharged.

3. Results and Discussion

The conventional and proposed converter structures are modelled in PSIM with their modulation techniques which are explained above. Modulation index is held at 1.0 for both operations. A resistance and inductance are used as load. The parameters are given: R=5Ω, L=50mH, and flying capacitors value=4400μF.

In order to obtain the rms value as 220 V at the output of inverter topologies, the voltages of DC link bus are selected as following: V_{dc} = 400 V, $V_1 = V_3$ = 100/3 V, and V_2 = 200/3 V.

The frequency of reference signal in PWM is chosen as 60 Hz and the carrier signals is 10 kHz. The output voltage and current of conventional topology is shown in Fig. 6, and the proposed topology's simulated waveforms are illustrated in Fig. 7. Table 2 shows the voltage THD values of each topology.

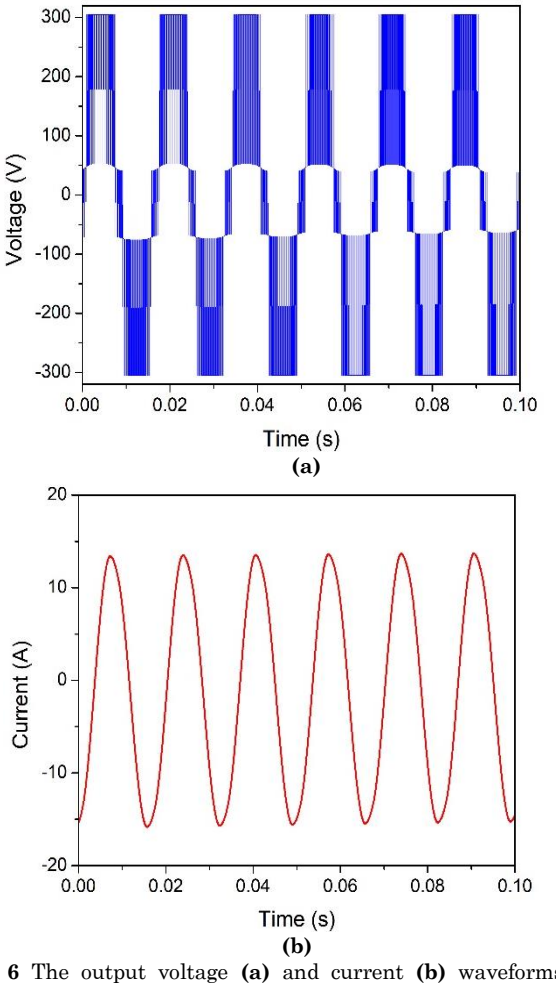

Fig. 6 The output voltage **(a)** and current **(b)** waveforms of conventional four-level topology.

The efficiency and THD values are significant parameters to evaluate a converter's performance. For this reason, the simulation results show that the THD value for proposed topology is reduced by 7.3% and the efficiency is raised by 2% in comparison with conventional configuration.

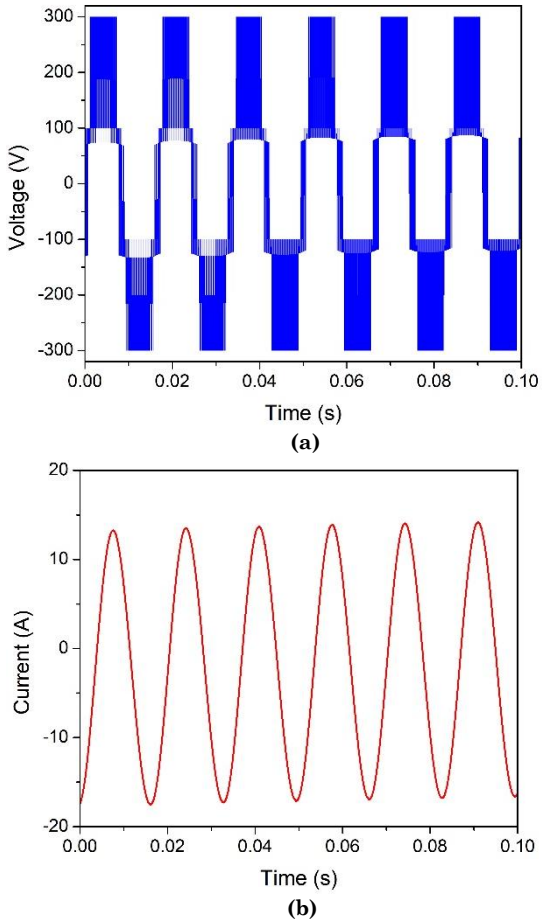

Fig. 7 The output voltage **(a)** and current **(b)** waveforms of proposed four-level h-bridge topology.

Table 2.
Efficiencies and Voltage THD values of topologies from simulation results.

Topology	Efficiency (%)	THD (%)
Conventional	81.03	45.37
Proposed H-Brdige	82.57	42.05

In the conventional topology, the load is inserted between the leg in which switches are connected and DC-link capacitors. This type of connection leads to low frequency circulating currents in the DC-link capacitors. However, the load is attached between the legs of switches in proposed topology in order to eliminate the low frequency circulating currents.

Since the voltage balancing issue is an important characteristic feature for flying-capacitor multilevel inverter topologies, the less number of capacitors for the clamping purpose is a desired property. While two flying capacitors are used totally in conventional topology, only one capacitor suffices in the proposed one.

Also, the simulation results show that the total magnitude of DC sources for inputs of topologies are different from each other. While the conventional topology needs a magnitude of 400 V DC for input source, a magnitude of 400/3 V DC input is enough for

proposed converter topology in order to have the same voltage magnitudes at the output of both configurations.

4. Conclusions

A comparison between conventional four-level flying capacitor topology and proposed four-level flying capacitor H-bridge topology is performed in this paper. The proposed converter configuration has some advantages, such as the same blocking voltages for all switches, unnecessariness of capacitor midpoint connection, and less number of flying capacitor.

In addition to these advantages of the h-bridge topology, it is observed that the THD value of the proposed topology displayed better performance than the conventional one. Also, the efficiency of this novel converter topology is increased by some amount.

As the future works of this proposed topology, the voltage balancing of flying capacitors can be examined in details. Also, a new study can be done to discover whether there are some advantages for the usage of this novel h-bridge topology in the converter applications of electrical or hybrid electrical vehicles.

Acknowledgments

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