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Six-Correction Logic (SCL) Gates in Quantum-dot Cellular Automata (QCA)

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Abstract *- Quantum Dot Cellular Automata (QCA) is a promising nanotechnology in Quantum electronics for its ultra low power consumption, faster speed and small size features. It has significant advantages over the Complementary Metal–Oxide–Semiconductor (CMOS) technology. This paper present, a novel QCA representation of Six-Correction Logic (SCL) gate based on QCA logic gates: the Maj3, Maj AND gate and Maj OR. In order to design and verify the functionality of the proposed layout, QCADesigner a familiar QCA simulator has been employed. The simulation results confirm correctness of the claims and its usefulness in designing a digital circuits.*

Keywords—*Quantum Cellular Automata; QCA Logic Gates; QCA Six-correction logic (SCL) gates.*

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I. INTRODUCTION

Quantum cellular automata (QCA) have been used widely to digital circuits and systems. QCA technology is a promising alternative to CMOS technology. It is attractive due to its fast speed, small area and low power consumption, higher scale integration, higher switching frequency than transistor based technology. QCA functions are based on Columbic interaction instead of current used in CMOS, so there is no leakage current. Additionally, it has major advantages such as low power consumption, high speed and small space consumption. QCA was presented in (Porod, W., 1997) for the first time and many sequential, combinational and reversible circuits have been introduced so far (Porod, W., 1997; Tougaw *et al.*, 1994; Wang *et al.* 2003; Zhang *et al.* 2005; Huang *et al.* 2007; Bhagyalakshmi *et al.* 2010; Sen *et al.* 2013; Bahar *et al.* 2013a; Bahar *et al.* 2013b; Islam *et al.* 2014; Bahar and Waheed 2014; Sarker *et al.* 2014; Bahar *et al.* 2015a; Bahar *et al.* 2015b). The basic structure in QCA is a cell that has four dots positioned at the corners of the squared cell and two free electrons. Each dot can be occupied by one of the two hopping electrons shown in figure 1.

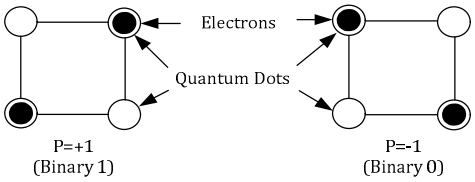

Figure 1. QCA cell and the two stable polarizations

Since the mutual behavior of the electrons is based on the Columbic interaction, they arrange themselves diagonally in order to reach to the maximum distance. Electrons can tunnel between dots through the barriers but cannot leave the cell; hence, there is no current flow. As shown in Figure 1 two stable polarization (p) states might occur, which represent the binary values “0” and “1”.

In order to implement gates and circuits, QCA benefits from Columbic interaction between cells. An array of cells that are aligned can construct a QCA wire which is shown in Figure 2. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force. Accordingly, QCA wires can be used to propagate information from one end to another (Kim *et al.*, 2007).

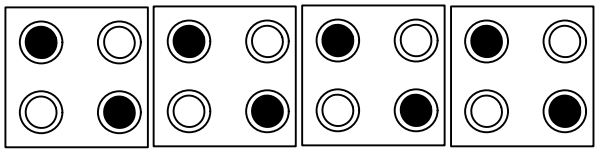

Figure 2. QCA wire

Two fundamental QCA gates are the inverter and the majority gate. Many structures are implemented based on these two gates like the AOI (Huang *et al.*, 2004), the complex gate (Townsend, W. J., & Abraham, J. A., 2004) and one bit QCA full adder (Kim *et al.*, 2007; Swartzlander, *et al.*, 2010; Sayedsalehi *et at.*, 2011). Figure 3 show three types of inverter gate; however, since the last one operates properly in all various circuits, it is used more in different designs

compared to the two other types. This inverter is made of four QCA wires. The input polarization is split into two polarizations and in the end, two wires join and make the reverse polarization.

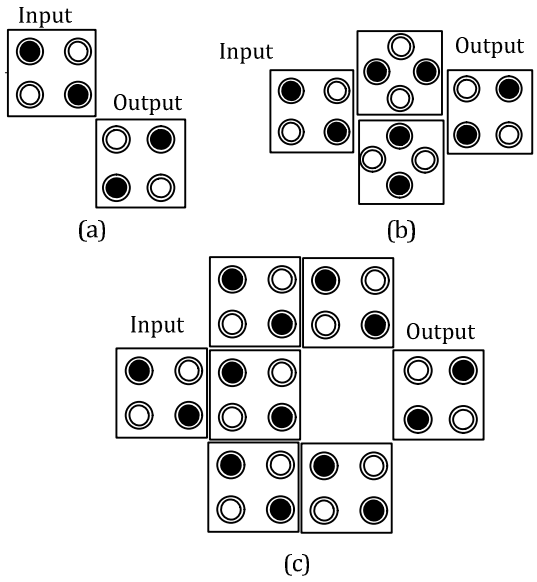

Figure 3. Three different structures of inverter gates

Majority gate consists of five cells, three inputs, one output and a middle cell shown in figure 4. The middle cell named device cell by reason of its function, switches to major polarization and determines the stable output. Majority gate can be programmed such that it functions as a 2-input AND or a 2-input OR by fixing one of the three input cells to p = -1 or p= +1, respectively. The Boolean expression of majority gate is as follows:

$$MV(A,B,C) = AB + AC + BC \qquad (1)$$

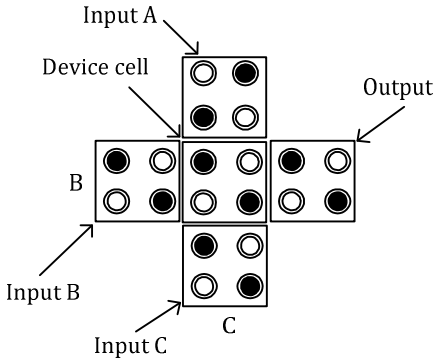

Figure 4. QCA majority voter gate

II. Proposed Circuit and Presentation

Six-Correction Logic Gate is a 4 x 4 gate with two garbage outputs (Bhagyalakshmi, *et al.*, 2010), the input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S) and output is defined by P = A, Q = B, R = C, S=A (B+C)⊕D the relation between input and output shown in figure 5. There is a one-to-one mapping between inputs and outputs of SCL gate and it can be used to add 6 to the sum in order to correct it to get the correct BCD sum (Bhagyalakshmi, *et al.*, 2010).

Theoretical implementation with sample input are given below

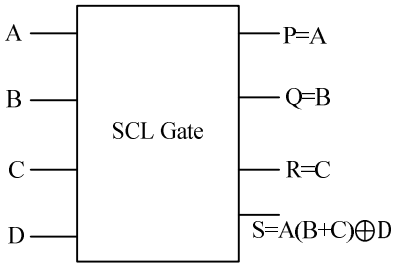

Figure 5. Six-Correction Logic gate

Figure 6 shows the QCA representation of Six-Correction Logic Gate (SCLG) based of majority voter (MV) gate. Here five majority gates are used to design Six-correction logic gate (SCLG).

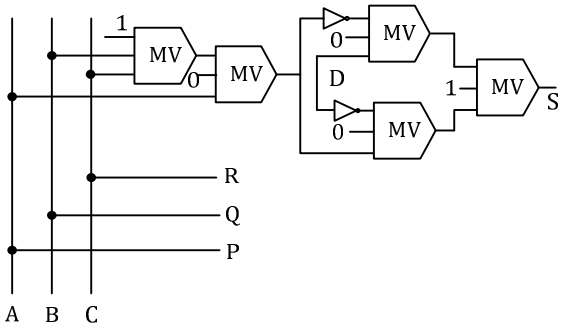

Figure 6. QCA block diagram of SCL gate

III. Simulation and Result Discussion

The circuit is functionally simulated using the QCADesigner (Walus *et al.*, 2004). The simulated circuit layout is shown in figure 6, here the input signals are: A, B, C and D and the output signals are: P=A, Q=B, R=C and S=A (B+C)⊕D and this module goes through four clock zones, it means that the delay is a full clock cycle. Therefore, at the output P, Q, R and S are available one clock cycles after A, B, C and D has been applied. Moreover, it requires sixty one (61) cells and total area of 0.095 μm^2.

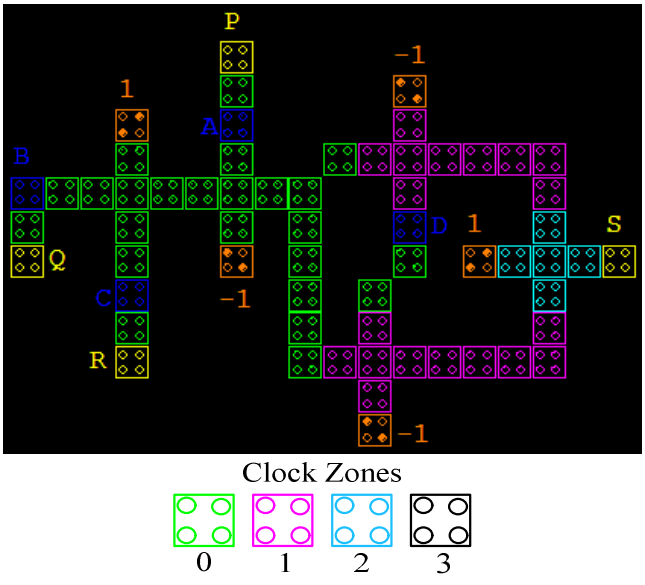

Figure 7. QCA circuit layout of Six-correction logic gate

A= 0, B=0, C= 0, D=0
S = (A (B+C) ⊕ D)
= (0 (0+0) ⊕ 0)
= (0 (0) ⊕ 0)
= (0 ⊕ 0)
= 0

A= 0, B= 0, C= 0, D=1
S = (A(B+C) ⊕ D)
= 0 (0+0) ⊕ 1
= 0 (0) ⊕ 1
= (0 ⊕ 1)
= 1

A=0, B=0, C=1, D=0
S = (A(B+C) ⊕ D)
= 0 (0 +1) ⊕ 0)
= 0 (1) ⊕ 0)
= (0 ⊕ 0)
= 0

A=0, B= 0, C= 1, D=1
S = (A(B+C) ⊕ D)
= 0 (0+1) ⊕ 1
= 0 (1) ⊕1
= (0 ⊕ 1)
= 1

A= 0, B=1, C=0, D=0
S = (A (B+C) ⊕D)
= 0 (1+0) ⊕ 0
= 0 (1) ⊕ 0
= (0 ⊕ 0)
= 0

A= 0, B=1, C=0, D=1
S = (A (B+C) ⊕D)
= 0 (1+0) ⊕1
= 0 (1) ⊕1
= (0 ⊕ 1)
=1

A= 0, B= 1, C= 1,D=0
S = (A(B+C) ⊕ D)
= 0 (1 +1) ⊕ 0
= 0 (1) ⊕ 0
= (0 ⊕ 0)
=0

A= 0, B= 1, C= 1, D=1
S = (A(B+C) ⊕ D)
= 0 (1+1) ⊕1
= 0 (1) ⊕1
= (0 ⊕ 1)
= 1

A=1, B = 0, C= 0, D=0
S = (A (B+C) ⊕ D)
= 1(0+0) ⊕ 0
= 1 (0) ⊕ 0
= (0 ⊕ 0)
= 0

A=1, B= 0, C= 0, D=1
S = (A(B+C) ⊕ D)
= 1 (0 +0) ⊕ 1
= 1 (0) ⊕ 1
= (0 ⊕ 1)
= 1

A= 1, B= 0, C= 1, D=0
S = A (B+C) ⊕ D)
= 1 (0 +1) ⊕ 0
= 1 (1) ⊕ 0
= (1 ⊕ 0)
= 1

A= 1, B= 0, C= 1, D=1
S = (A (B+C) ⊕ D)
=1 (0 +1) ⊕ 1
= 1 (1) ⊕ 1
= (1 ⊕1)
= 0

A= 1, B= 1, C= 0, D=0 S = (A (B+C) ⊕ D)
= 1 (1 +0) ⊕ 0
= 1 (1) ⊕ 0)
= (1 ⊕ 0)
= 1

A= 1, B= 1, C= 0, D=1
S = (A(B+C) ⊕ D)
= 1 (1 +0) ⊕
= 1 (1) ⊕ 1
= (1 ⊕ 1)
= 0

A= 1, B= 1, C= 1, D=0
S = (A (B+C) ⊕ D)
= (1 (1 +1) ⊕ 0)
= 1 (1) ⊕ 0
= (1 ⊕ 0)
= 1

A= 1, B= 1, C= 1, D=1
S = (A(B+C) ⊕ D)
= 1 (1 +1) ⊕1
= 1 (1) ⊕ 1
= (1 ⊕ 1)
= 0

We can find the output value of S is low level when the input digits (A = 0, B = 0, C = 0, D = 0) and S is up level when the input digits (A = 0, B =0, C= 0, D =1). We look into the other two output values of A, B and C also translating the input data successfully. The simulated waveforms of SCL gate is shown in figure 8. Here, the S output is delayed by 0.75 clock cycle. Finally, in Table 1, designing parameters are compared.

Table 1. Designing parameters of proposed SCL gate

Parameter	Value
Number of cells	61
Covered area (μm^2)	0.095
Clock used	3
Time delay (clock cycle)	0.75

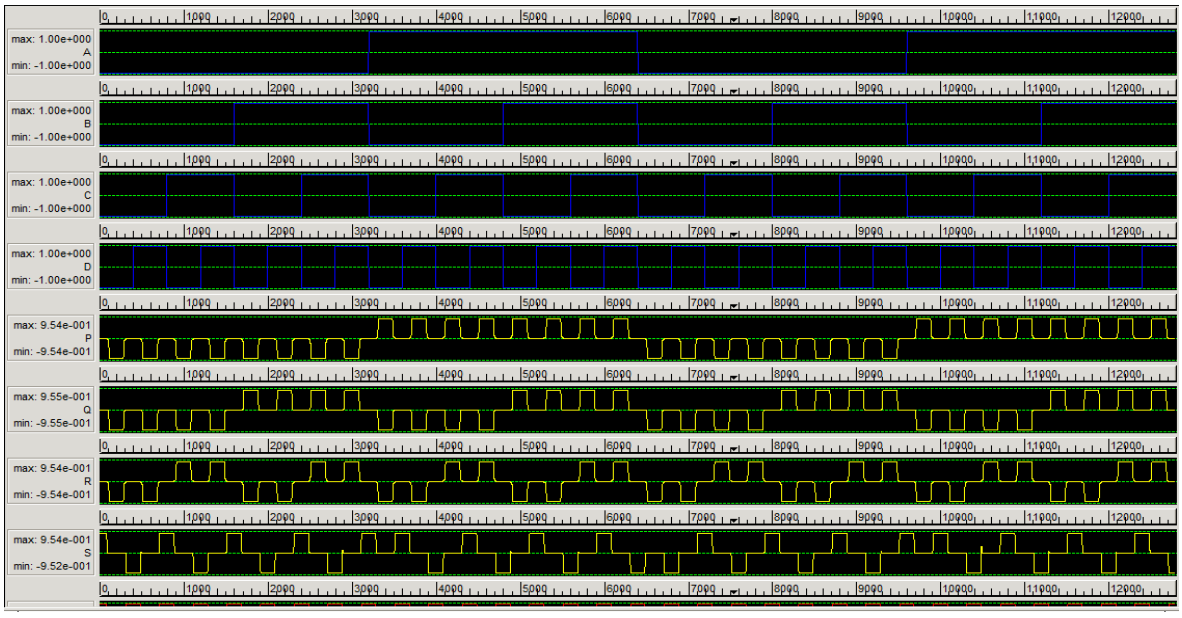

Figure 8. Simulated waveforms for Six-correction logic gate (SCLG) circuit

IV. CONLUSIONS

This paper present Six-correction logic (SCL) gate based on QCA does logic gates. The proposed SCL gate has been simulated and verified using QCADesigner. The result is compared in terms of complexity (cell count), covered area and time delay. The simulation result shows that the proposed design achieves a sound improvement. This design will be very helpful for designing ultra low power digital circuits.

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